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Third Semester B.E. Degree Examination, Jan./Feb. 2023 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram, explain basic operational concepts of computer. (10 Marks)
b. Illustrate Instruction and Instruction sequencing with an example. (10 Marks)

OR

- 2 a. How to measure the performance of a computer? Explain. (08 Marks)
b. Explain the 3-address, 2-address and 1-address instruction with an example. (06 Marks)
c. Explain system software functions in computer. (06 Marks)

Module-2

- 3 a. What is an addressing mode? Explain any four types of addressing modes with example. (10 Marks)
b. Define subroutine and parameter passing. Explain how to pass the parameter by value and by reference. (10 Marks)

OR

- 4 a. What are assembler directives? Explain any five assembler directives. (10 Marks)
b. Explain shift and rotate operations with example. (10 Marks)

Module-3

- 5 a. With relevant diagram, discuss, implementation of interrupt priority using individual interrupt request. (06 Marks)
b. Explain the following: i) Vectored interrupts ii) Simultaneous requests. (08 Marks)
c. Write a note on registers in DMA interface. (06 Marks)

OR

- 6 a. Define interrupt, point out and explain various ways of enabling and disabling interrupts. (08 Marks)
b. Write a program to read a line from the keyboard and display it. (06 Marks)
c. Define bus arbitration. Explain centralized arbitration mechanism in DMA with a neat diagram. (06 Marks)

Module-4

- 7 a. With a neat diagram, explain internal organization of 16×8 memory chip. (10 Marks)
b. With a neat diagram, explain the working principle of magnetic disk. (06 Marks)
c. What are the major functions of disk controller? (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, $42+8=50$, will be treated as malpractice.

OR

- 8 a. With a neat diagram, explain internal organization of a $2M \times 8$ dynamic memory chip. (08 Marks)
- b. With a neat diagram explain a single-transistor dynamic memory cell. (06 Marks)
- c. Discuss the concept of cache memory. (06 Marks)

Module-5

- 9 a. With a neat diagram, explain single bus organization of the data path inside a processor. (08 Marks)
- b. Discuss the control unit organization of hard wired control. (06 Marks)
- c. With a neat diagram, explain microprogrammed control unit design. (06 Marks)

OR

- 10 a. Explain three bus organization of the data path. (08 Marks)
- b. Discuss the control sequence for execution of instruction ADD (R3), R1. (06 Marks)
- c. Draw and explain organization of the control unit to show conditional branching in the micro program. (06 Marks)
